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U.S. PATENT AND TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Shibaek Nam; Oseob Jeon; and Chulho Heo
Assignee: Fairchild Semiconductor Corporation
Title: Semiconductor Device Having Multi-Chip Package Structure
Application No.: 10/038,714 Filing Date: January 2, 2002
Examiner: Unknown Group Art Unit: 2811
Docket No.: M-11590 US Conf. No.: 8922

San Francisco, California
October 24, 2002

COMMISSIONER FOR PATENTS
Office of Initial Patent Examination
Customer Service Center
Washington, D.C. 20231

REQUEST FOR CORRECTED FILING RECEIPT

Dear Sir:

Applicants hereby request the Commissioner For Patents to correct the Official Filing Receipt for the above-identified patent application as follows:

- 1. Correct the Filing Date
- 2. Correct Inventor Name
- 3. Correct Title
- 4. Correct information referencing related case
- 5. Correct Attorney Docket Number

INVENTOR(S) NAME(S) OR ATTORNEY'S NAME(S) OR AGENT'S NAME(S)

Application No. 10/038,714

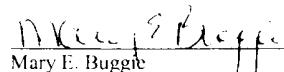
The first inventor's name has a typographical error. The inventor's name should read as Shibaek Nam. The Official Filing Receipt presently incorrectly reflects this inventor's name as Shiback Nam (emphasis added).

Because this was not an error on the part of Applicants, Applicants believe no fee is required.

Attached is a copy of the Filing Receipt having the above error and the change noted thereon, as well as copies of the first page of the patent application and Declaration for Patent Application and Power of Attorney. Therefore, it is respectfully requested that a corrected Filing Receipt be issued.

If this action does not lead to issuance of a corrected Official Filing Receipt as requested, please contact the undersigned at (415) 217-6000.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on October 24, 2002.


Mary E. Buggie

10/24/02
Date of Signature

Respectfully submitted,



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UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING DATE	GRP/ART UNIT	FILED REC'D	ATTY/BOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
10/038,714	01/02/2002	2811	1880	M-11590 US	4	60	8

CONFIRMATION NO. 8922
FILING RECEIPT


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Date Mailed: 03/18/2002

SKJERVEN MORRILL MACPHERSON LLP
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Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s) **ShibaeK**
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Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 03/15/2002

Projected Publication Date: 07/03/2003

Non-Publication Request: No

Early Publication Request: No

Title

Preliminary Class

257

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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U.S. GOVERNMENT
PRINTING OFFICE

SEMICONDUCTOR DEVICE HAVING MULTI-CHIP PACKAGE STRUCTURE

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Inventors: Shibaek Nam
Oseob Jeon
Chulho Heo

10 FIELD OF THE INVENTION

The present invention relates to semiconductor devices, and more particularly, to a semiconductor device having a multi-chip package structure.

BACKGROUND

15 Multiple integrated circuit ("IC") chips can be combined in a single package for some applications of semiconductor devices. These are generally referred to as "multi-chip packages." For example, in a power semiconductor device, a smart power switching ("SPS") product may contain a control IC chip, which is a driving device, and a transistor chip, which is a switching device, mounted together horizontally on a lead frame, which must be large enough to accommodate both chips side-by-side. During a packaging process, a common method for insulating a multi-chip package is to attach one chip to the lead frame by inserting a ceramic plate or epoxy mold compound ("EMC") plate between die adhesives or to use a liquid non-conductive adhesive, such as an epoxy. However, there are manufacturing problems with this method.

20 25 30 Inserting a ceramic plate or an EMC plate between die adhesives is problematic. First, the ceramic plate is breakable and expensive, so the manufacturing cost increases. Second, the overall packaging process is made more complicated since several additional steps are required. These steps include inserting the ceramic or EMC plate and curing to harden the die adhesives. Third, the overall packaging process is not only complicated but also is likely to cause faults in a die adhesive, such as void, delamination, and die tilt. Such faults in a die adhesive lower product yield rate and product reliability. The product